F16.1

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Application Note
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Programmable Interval Timer and Counter for Use with RCA COSMAC Development Systems

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This Note describes a programmable interval timer and counter for use with RCA COSMAC Development Systems CDP18S001, CDP18S002, and CDP18S004 hardware. The CDP18S001 and CDP18S002 utilize the RCA CDP1801 COSMAC Microprocessor; the CDP18S004 utilizes the CDP1802. The information given and the terminology used are based on the assumption that the reader is familiar with the COSMAC Development Systems manuals.

Circuit Capabilities

The circuit for the programmable timer-counter is given in Fig. 1(a) and (b). It includes two main sections: a) a controller that allows the user to select various clock rates and various means of signalling the CPU after a given count, and b) an interval timer which is a presettable down counter. Table I gives the interconnect information for the interval timer and the controller. This unit can be used in one- or two-level I/O systems. The controller is programmed by a single output instruction with the bit pattern in M[R(X)] specifying the commands and their destination. The interval timer is accessed as two consecutive bytes in upper memory.

This timer unit permits its users to set the timer clock rate, count external events, and signal the CPU at preset intervals. Programmable options are:

- Clock rate, selectable from 131.3 μs to 16.804 ms in multiples of 131.3 μs. Faster rates, up to the machine cycle time, are possible with simple wiring modifications.
- Repeated timeout pulses at the above rates, or a single programmed timeout to a maximum of 18.35 minutes.
- Choice of setting an external flag and interrupt at timeout, or just an external flag.
- External counter input for positive- or negative-going inputs allowing counts up to 65,536.
- Buffered timeout output which can be used to signal an external device after a preset interval.

Table I – Interconnect List for Timer To Controller and COSMAC Development System

Timer Circuit	CDS Hardware		Signal
Pin	Slot	Pin	Name
1	*		SELA1-P
2	*		SELA3-P
3	14	3	A15-P
4	14	4	A14-P
5	14	5	A13-P
6	14	6	A12-P
7	14	7	A11-P
8	14	8	A10-P
9	14	9	A9-P
10	14	10	A8-P
11	13	11	DI0-N
12	13	12	DI1-N
13	13	13	DI2-N
14	13	14	DI3-N
15	13	15	DI4-N
16	13	16	DI5-N
17	13	17	DI6-N
18	13	18	DI7-N
19	Cont.	9	TIMER CLOCK-P
20	14	20	*ADS-P
B	*		SELA2-P
C	13	C	DO0-N
D	13	D	DO1-N
E	13	E	DO2-N
F	13	F	DO3-N
H	13	H	DO4-N
J	13	J	DO5-N
K	13	K	DO6-N
L	13	L	DO7-N
M	13	M	A7-P
N	13	N	A6-P
P	13	P	A5-P
R	13	R	A4-P
S	13	S	A3-P
T	13	T	A2-P
U	13	U	A1-P
V	13	V	A0-P
W	13	W	MWR-P1
X	Cont.	7	CARRY-N
Y	+5 V		V_{DD}
Z	GND		GND

*Assigned per Table II

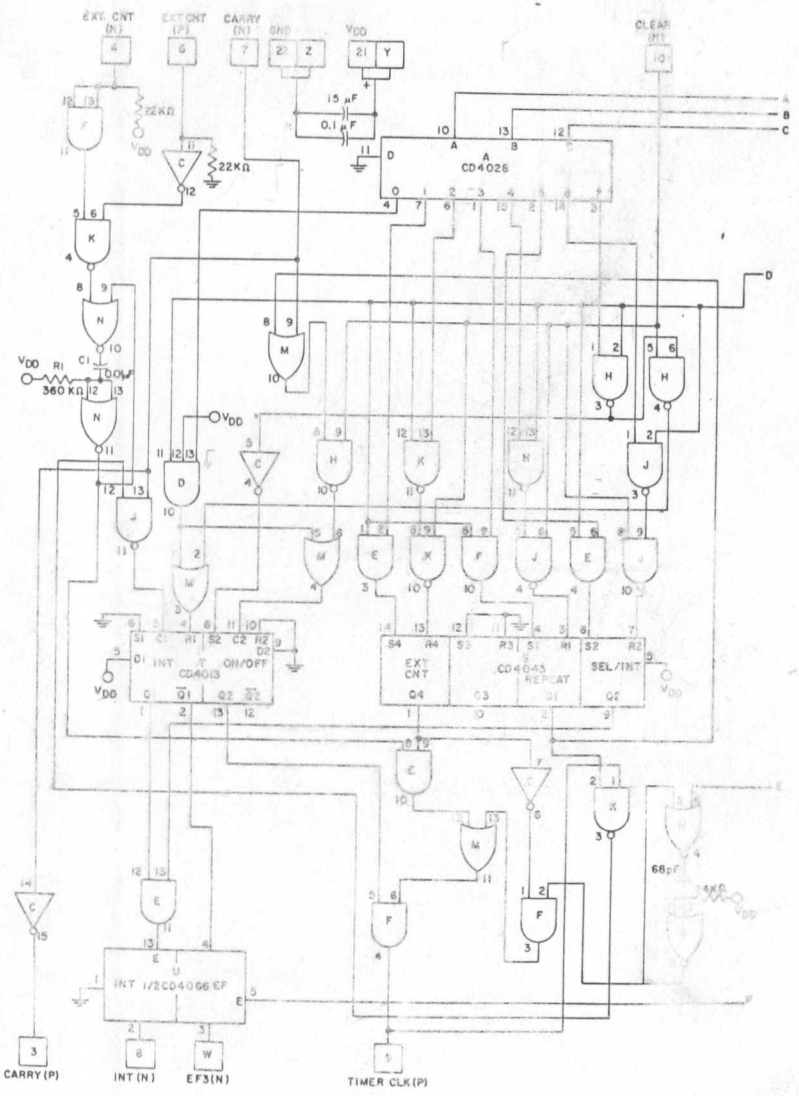


Fig. 1(a) – Circuit and logic diagram of controller for programmable timer-counter. (Part 1)

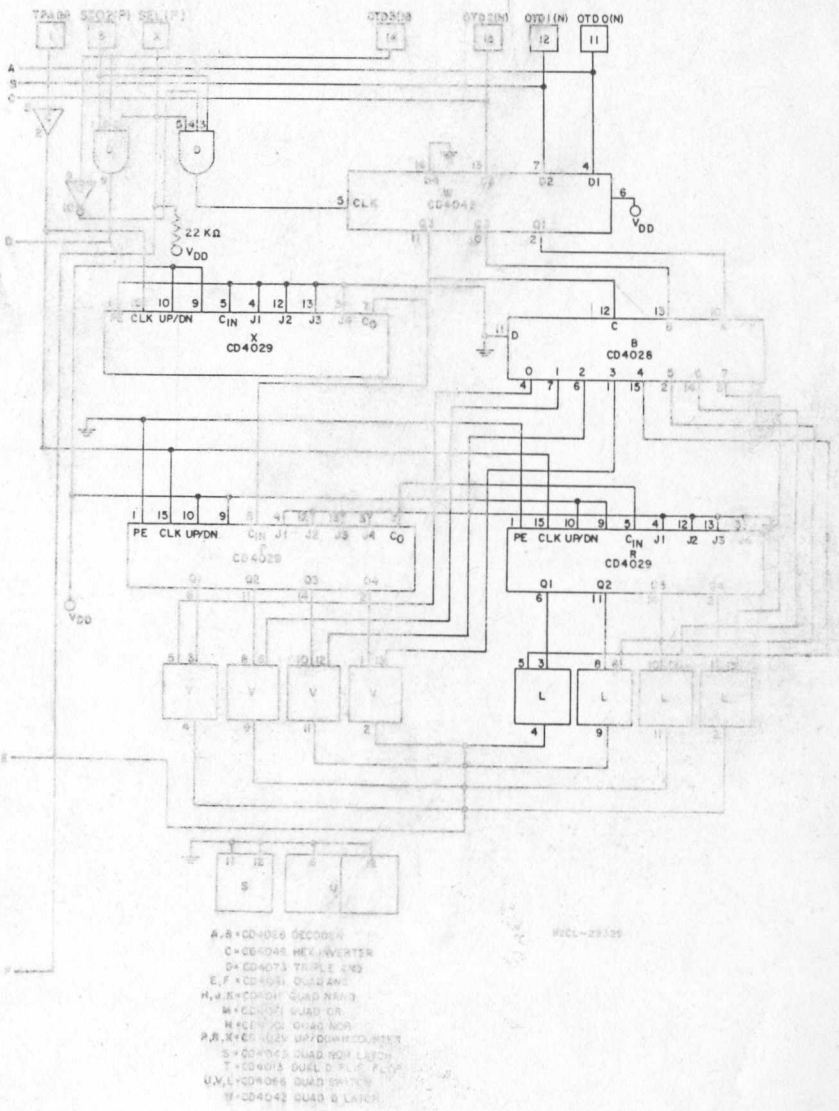


Fig. 1(a) – Circuit and logic diagram of controller for programmable timer-counter. (Part 2)

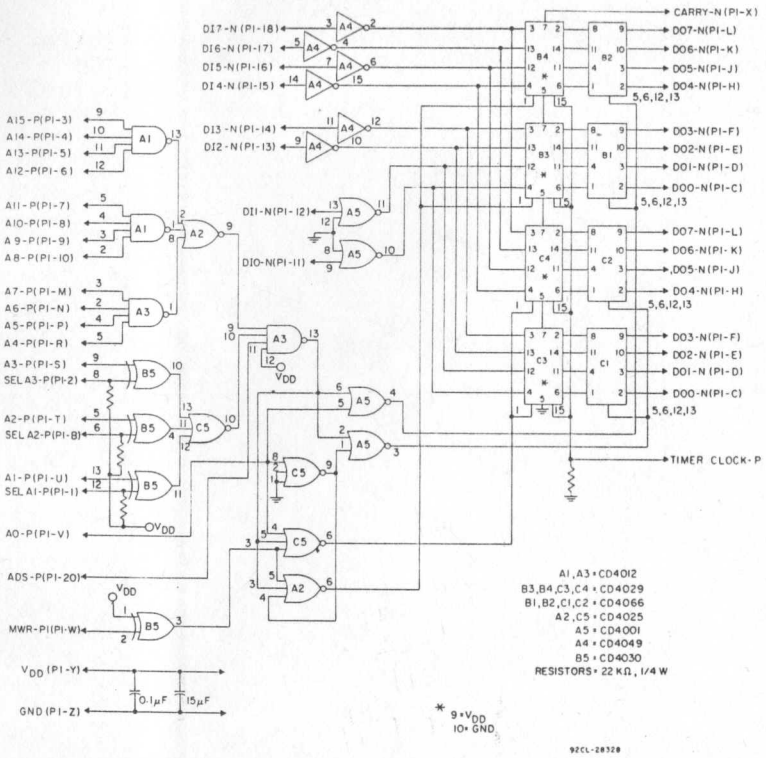


Fig. 1 (b) – Circuit and logic diagram of interval timer of programmable timer-counter.

The timer logic is implemented so that, when the timer is loaded from software, the hexadecimal value should be used; but, when the timer's contents are read, the **complement** of the accumulated count is obtained. This arrangement is advantageous in counting applications, as well become apparent in Example 4.

The external count input fires a one-shot of approximately 2.7 ms to minimize noise problems. Although this value limits the external clock input to about 180 kHz, the time constant can easily be changed to suit individual application needs by modifying C_1 and R_1.

When the timer is used in a two-level I/O system, Pin X must be high to select the timer control. This pin can be left open for one-level systems because it is pulled up on the card.

Addressing

The timer appears as two bytes in upper memory location 'FFFZ' where 'Z' is an address selection wired in accordance with Table II. The high-order byte of the timer is associated with the higher address number.

Table II – Signal Levels to Control Memory Address Assignments

	Pin 1 (SELA1-P)	Pin B (SELA2-P)	Pin 2 (SELA3-P)
FFF0,1	L	L	L
FFF2,3	H	L	L
FFF4,5	L	H	L
FFF6,7	H	H	L
FFF8,9	L	L	H
FFFA,B	H	L	H
FFFC,D	L	H	H
FFFE,F	H	H	H

Commands

Two sets of commands are recognized, depending on whether bit 3 of M[R(X)] is a one or zero. If bit 3 = 1, the commands are used to select a clock rate. If bit 3 = 0, the commands are used to set the options for a count or timeout. Tables III and IV list these commands.

Table III – Summary of Controller Commands

	Set Clock Rate*								6N (1≤N≤7)+
Bit #	7	6	5	4	3	2	1	0	
M(R(X)) =	X	X	X	X	1	X	X	X	RATE SET INSTRUCTIONS
					1	0	0	0	131.3 μs
					1	0	0	1	262.6 μs
					1	0	1	0	525.1 μs
				not	1	0	1	1	1.050 ms
					1	1	0	0	2.100 ms
				used	1	1	0	1	4.201 ms
					1	1	1	0	8.402 ms
					1	1	1	1	16.804 ms

Note: Outputs of 8.2 μs, 16.4 μs, 32.8 μs, and 65.6 μs are available at output connection 'X'. Any or all of them may be used in place of output connections 'P' or 'R'.

	Set Options*								6N (1≤N≤7)+
M(R(X)) =	X	X	X	X	0	X	X	X	ACTION
					0	0	0	0	Disable clock output, reset external flag, interrupt FF.
					0	0	0	1	Select external count input as clock.
				not	0	0	1	0	Select divide-down option for clock rate set above.
					0	0	1	1	Select repeated timeouts at clock rate set above.
				used	0	1	0	0	Select single, count-down timeout, not repeated.
					0	1	0	1	Select interrupt and external flag at timeout.++
					0	1	1	0	Select external flag only at timeout.
					0	1	1	1	Enable clock output, reset external flag, interrupt FF.

* Assumes controller has been selected with appropriate output instruction and device number, or one-level I/O system is being utilized.

\+ Same N assumed for both clock rate and options programming.

++ Once the interrupt flip-flop is set, it can be reset only by command 00 or machine clear.

Table IV – Controlling Commands For Specific Options

Option	Enable Command	Disable Command
Clock Output	1) 07 command	1) 00 command 2) Machine clear 3) Timeout† (without repeat option)
External Count	1) 01 command	1) Machine clear 2) 02 command
Repeat/Divide	1) 03 command	1) Machine clear 2) 04 command
Interrupt-Flag*	1) Timeout†	1) 07 command 2) Machine clear 3) 00 command
Interrupt at Timeout	1) 05 command	1) Machine clear 2) 06 command

† Change of state triggered on leading edge of signal.

* For two-level I/O system, controller must be selected before external flag can be sampled by program.

Timeout Event Actions

At the conclusion of a timeout or counting sequence, the following actions occur.

For the single count-down timeout option, the circuit sets the external flag, generates an interrupt if selected, and disables further clock output.

For the repeated timeout option, the circuit sets the external flag and generates an interrupt if selected.

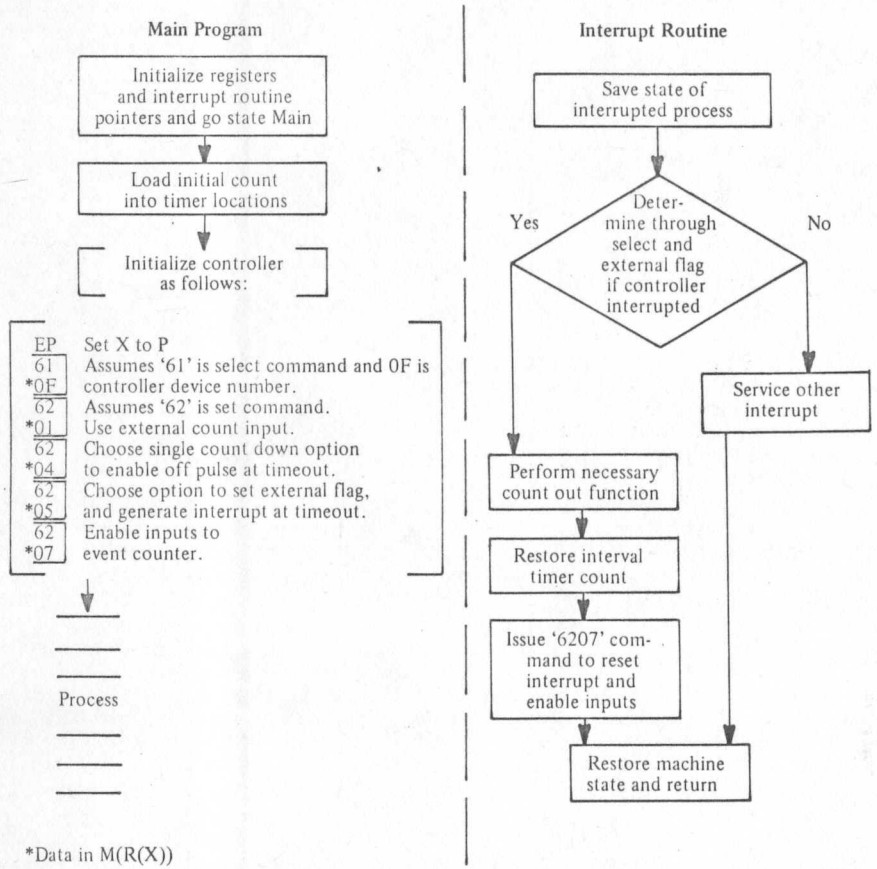
Machine Clear-State Results

When the reset button is actuated, the following actions occur. The clock output is disabled, the external flag is reset, the interrupt is reset, the external flag only is set at timeout, the divide-down clock option is selected, and the single count-down time-out option is selected.

Examples

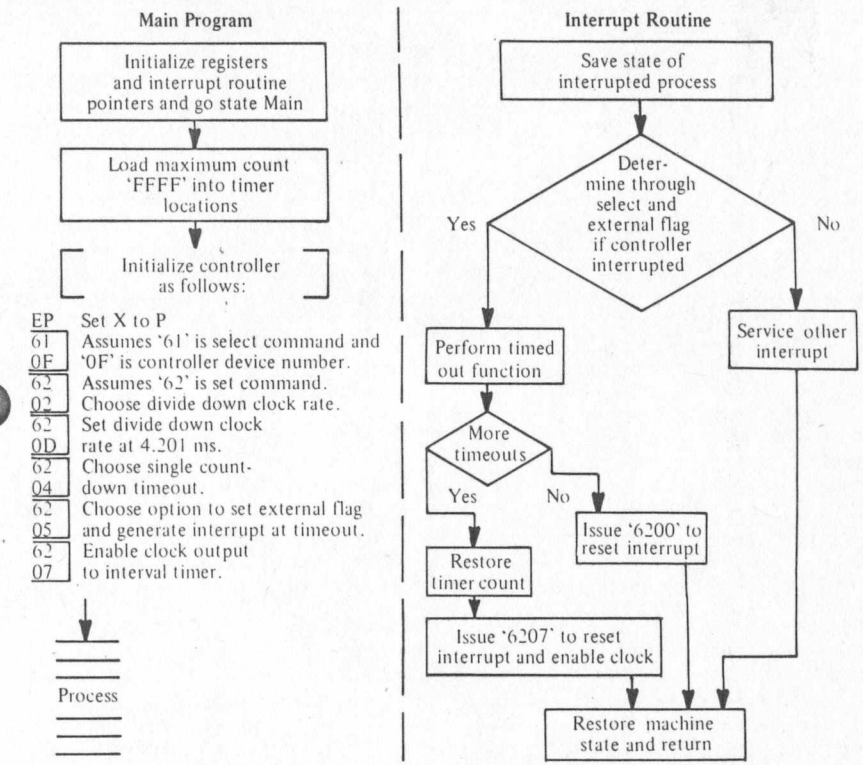
Following are four sample programs.

Example 1. Use timer to count external events to a specific number and then generate an interrupt.

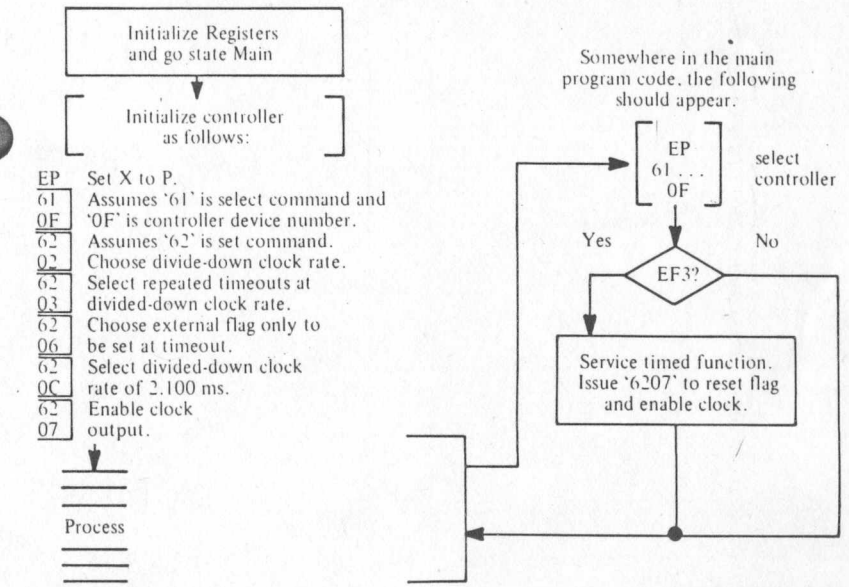


*Data in M(R(X))

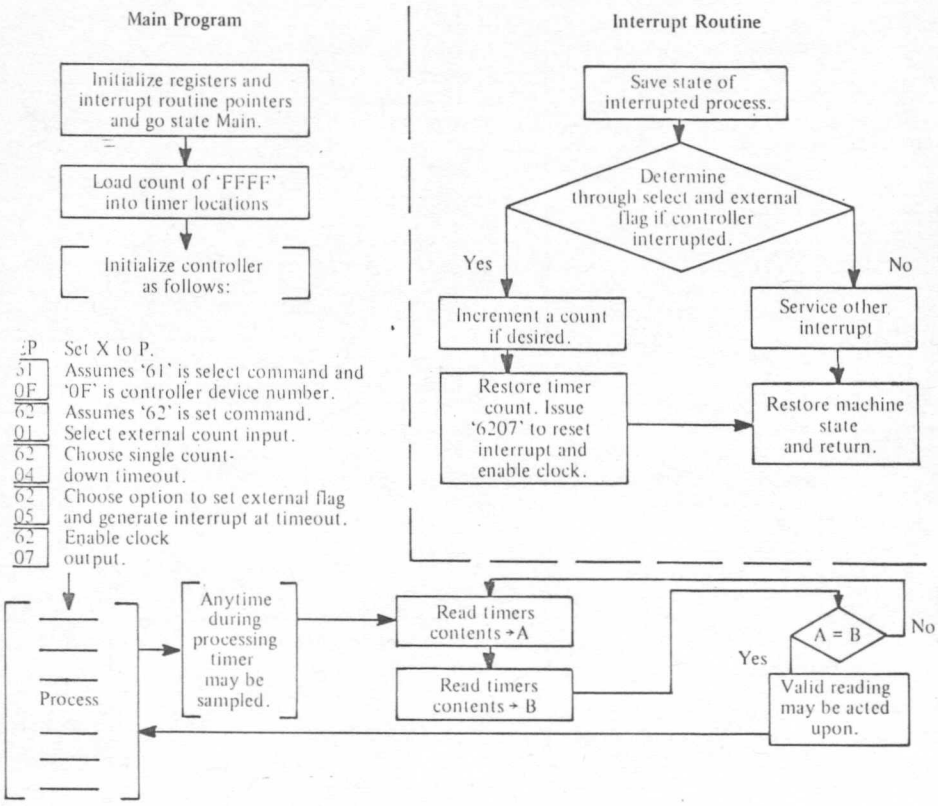
Example 2. Set up timer and controller to timeout, and generate an interrupt in 4.59 min.



Example 3. Utilize controller to generate repeated timeout at divided-down clock rate of one every 2.1 milliseconds. Do not, however, generate an interrupt at timeout. External flag will be sampled when convenient in main program.



Example 4. Count events and accumulate sum in timer to a maximum of 65,536. In this case timeout is not wanted unless entire count is exhausted. Sum can be sampled in program by examining timer locations. Timer should be initialized to X'FFFF' which, when read back in complemented form, will appear as X'0000'. The first count will decrement X'FFFF' to X'FFFE' and if accessed by program will correctly be read as X'0001'. When the timer's contents in this mode (clock not synchronized with machine instructions) are examined, the reading should not be considered valid until two consecutive accesses yield the same value.



Loading the Counter

The following program shows how to load an initial value into the counter.

Instruction	Comments
F8 XX	Load high-order byte of count into D
53	Store into high-order byte of counter; assumes R(3) = FFFZ where Z = 1,3,5,7,9, B,D,F corresponding to the timer's address.
23	Decrement R3
F8 XX	Load low-order byte of count into D
53	Store into low-order byte of counter.